

ELID EL-80 AND ES-550 FRONT END PROCESSOR CONFIGURATION GUIDE

WHAT IS AN EL-80 ?

EL-80 is an intelligent front-end processing system for commanding a cluster of up to 64 ELID door access controllers such as EL-22XX, EL-12XX etc.

The motherboard was based on the new CPU-97 16-bit single board computer.

The system is generally referred to as the Readers Processing Unit (Acronym : RPU).

WHAT IS AN ES-550 ?

ES-550 is another intelligent front-end processing system for commanding a cluster of up to 64 ELID Input/Output Field Devices, such as EFD-80 etc.

The motherboard was also based on latest CPU-97 16-bit single board computer.

The system is generally referred to as Data Gathering Panel (Acronym : DGP).

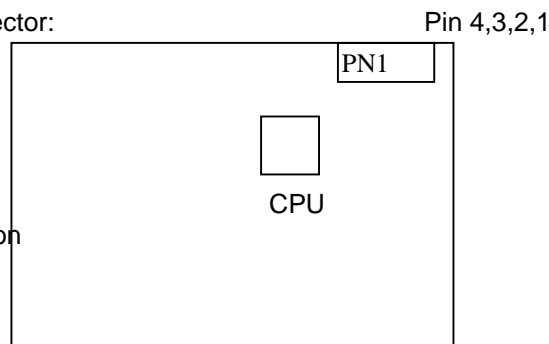
POWERING UP THE UNIT

The motherboard, CPU97, is running a high speed 16-bits microprocessor and equipped with 1Mega Byte of memory chips. The CPU (central-processing unit) runs at clock rate of 24 MHz. It requires good power supply regulation and noise suppression. Only good quality power supply (switch mode or linear mode) with an output voltage of 12VDC rated at 1.5A and noise margin below that of 10dB should be used in all cases.

Connect 12VDC supply to PN1 connector:

Pin 1 : 12VDC
Pin 2 : GND
Pin 3 : GND
Pin 4 : 12VDC

You can use either Pin 1,2 combination or Pin 3,4 combination.
Remember Pin 1 and Pin 4 are common , so are Pin 2 and Pin3.



ROM (Read Only Memory)

The SYSTEM ROM contains the firmware and are supplied in a set of 2 chips, labelled as 'EVEN' and 'ODD'.

The 'EVEN' ROM chip should be inserted in IC socket U18.

The 'ODD' ROM should be inserted in IC socket U19.

You should be aware of the Firmware Title and the ROM Version number.

You would need to supply such information to ELID technical support and service staff.

The firmware title should be:

RPU for	EL-80
DGP for	ES-550

Note : Please remove the 12VDC power before removing the ROM set.

DIP SWITCH SETTINGS ON THE MOTHERBOARD

You will find only one DIP Switch on the board, labelled **SW2**.

It should be set to the following positions:

<u>ON</u>	<u>OFF</u>
Pin 1 : Cold Start	Normal
Pin 2 : Auto Mode	Auto OFF
Pin 3 : N/A	N/A
Pin 4 : N/A	N/A

COLD STARTING THE SYSTEM

You would need to execute COLD-START sequence for the FEP when you power up the system for the very first time, or you intended to erase off the data memory and reset configuration settings to default value, and or whenever the system experienced misbehaviour due to a possible corruption in the data memory.

Follow the COLD-START sequence below:

1. Set DIP Switch SW2, pin 1 position to ON (Cold-Start).
2. Press the RESET button (labelled SW1 on the board).
3. Wait for the RED LED (LD2) to do a quick THREE times blink and then settles down in a normal ONE second blinking interval.
4. That indicates COLD-START sequence has been completed.
5. Set DIP switch SW2, pin 1 position back to OFF (Normal).

SYSTEM RE-SET

You can, at any time, press the RESET switch (SW1) to re-set the system. That re-set will not destroy FEP's data memory and system configuration settings as long as pin 2 of DIP switch is set to an OFF position (Normal).

CPU WATCHDOG

CPU WATCHDOG is a special circuit designed to monitor and protect the CPU from the possibility of system locked up due to any hardware or software faults. You must enable the CPU WATCHDOG function in order for the circuit to work. The default factory setting is OFF.

Please ensure that jumpers are inserted in JP1: One across Pin 1 and Pin 2 and another across Pin 2 and Pin 3.

HOST PC COMMUNICATION PORT

The FEP is in turn connected to a PC (personal computer) designated as a POLLING STATION via a common RS232C cable.

Please connect a 3-4 wire shielded data cable between the PC's COM port and CN3 port located on the right hand top corner of the CPU-97 motherboard.



**CN3 (nearest to battery)
(9 pin DB9 male)**

Communication Cable Wiring Scheme

<u>PC (DB9)</u>	<u>CPU-97</u>
Pin 2	Pin 3
Pin 3	Pin 2
Pin 5	Pin 5
Pin 6,7 and 8 (wired together)	

Important Note

* Pin 6(DSR), Pin 7 (CTS) and Pin 8 (RTS) must be common on the PC COM side because the PC uses hardware handshaking protocol, otherwise the communication link between the PC and FEP will be broken.

TERMINAL PORT

You can connect a dumb terminal or a PC running terminal software to the Terminal Port on the CPU-97. The port is labelled as CN2 which is a DB9 connector, located below CN3 port.

Use a similar cable described above to link a terminal to port CN2.

The PC port used for terminal connection must be set to the following configuration:

BAUD	9600
DATA	8 bit
STOP	1
PARITY	None

INPUT POINTS CONFIGURATION

There are 16 channels of opto-coupler input ports available on the FEP motherboard (RPU or DGP). The input point connectors are labelled as CN10, CN11 and CN12 and the channel numbers are clearly labelled on the board.

<u>Connector</u>	<u>Description</u>	<u>Remark</u>
CN10	Inputs channel #1 to #8	(-End of the opto-coupler)
CN11	Inputs channel #9 to #16	(-End of the opto-coupler)
CN12	V+	(+End of the opto-coupler)
	12V	(12VDC supply)
	GND	(DC Ground)

Example for input connections,

1. To wire-up input 1 to Normally Open (NO) relay contact:
 1. Connect the NO port of the relay to input 1.
 2. Connect the COM (common) line of the relay to the GND point of the CPU-97 board.
 3. Connect the V+ line on the CN12 to 12V (also available on CN12).

OUTPUT POINTS CONFIGURATION

CPU-97 supports up to two ELID ES-8A external 8-relays boards for a total of 16 output relays.

The first ES-8A relay board is to be connected to CN4 connector on the CPU-97 board and the second ES-8A board goes to the CN9 connector.

Note:

CN4 is always designated as OUTPUT port number 1 to 8 and CN9 is always designated as OUTPUT port number 9 to 16.

SYSTEM PLUG-IN CARDS

CPU97 supports 4 card slots : SK1 , SK2 , SK3 and SK4.

SK1, SK2 must be inserted with ELID's EPCB16552 DUAL-CHANNEL SERIAL COMMUNICATION CARD.

SK1's EPCB16552 Card will be used for the BUS1 and BUS2 of the Reader/Field Devices loop.

SK2 EPCB16552 Card will be used for the BUS3 and BUS4 of the Reader/Field Devices loop.

Note : One BUS can drive up to 16 readers or Field Devices in a loop.

EPCB16552 DUAL CHANNELS SERIAL COMMUNICATION CARD SETTINGS

EPCB Board Located at SK1

SW2 (Port address)

Pin 1	ON
Pin 2	ON
Pin 3	OFF
Pin 4	OFF

SW1 (IRQ level)

Pin 1	ON
Pin 2	OFF
Pin 3	OFF
Pin 4	OFF

Note : For Revision 1 board, SW3 and SW4 must be All ON (with jumpers). Subsequent revision has abolished SW3 and SW4.

EPCB Board Located at SK2**SW2**

Pin 1	OFF
Pin 2	OFF
Pin 3	ON
Pin 4	ON

SW1

Pin 1	OFF
Pin 2	ON
Pin 3	OFF
Pin 4	OFF

Note : For Revision 1 board, SW3 and SW4 must be All ON (with jumpers). Subsequent revision has abolished SW3 and SW4.